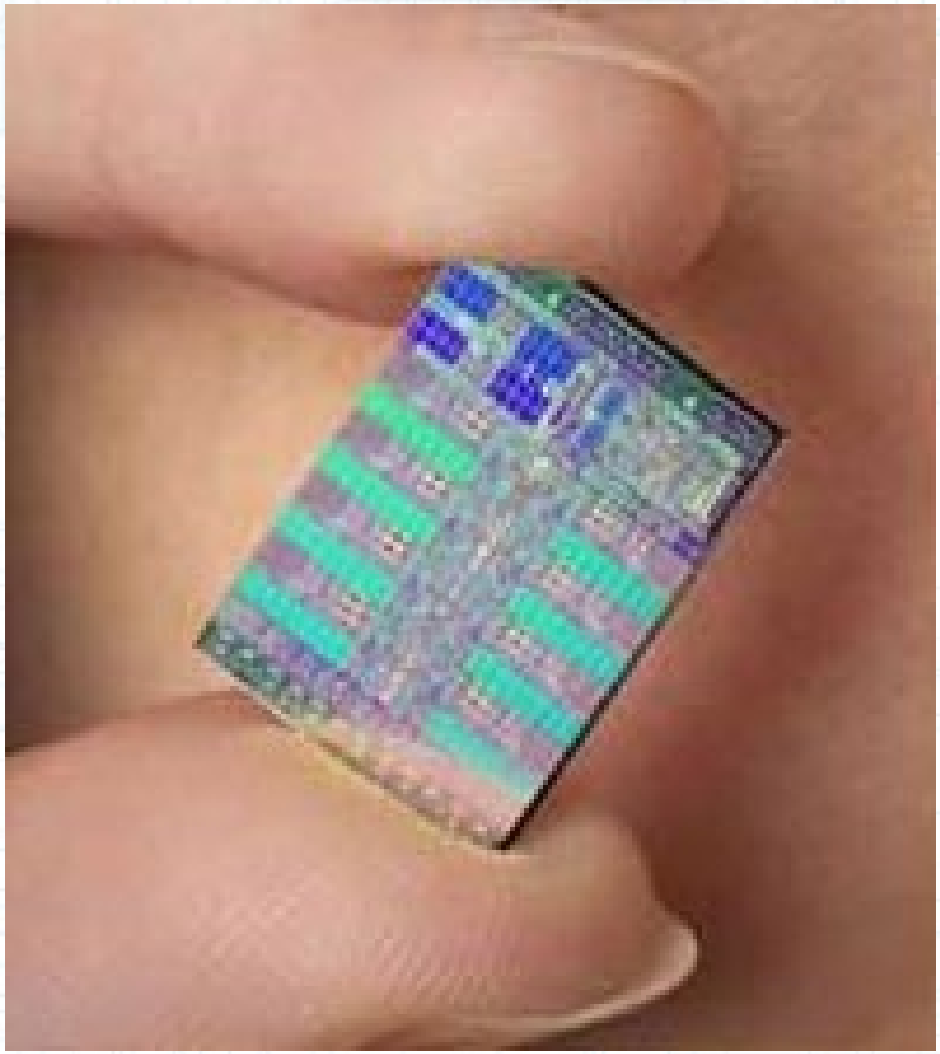

Cell Broadband Engine Architecture Processor

Ryan Layer
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SONY

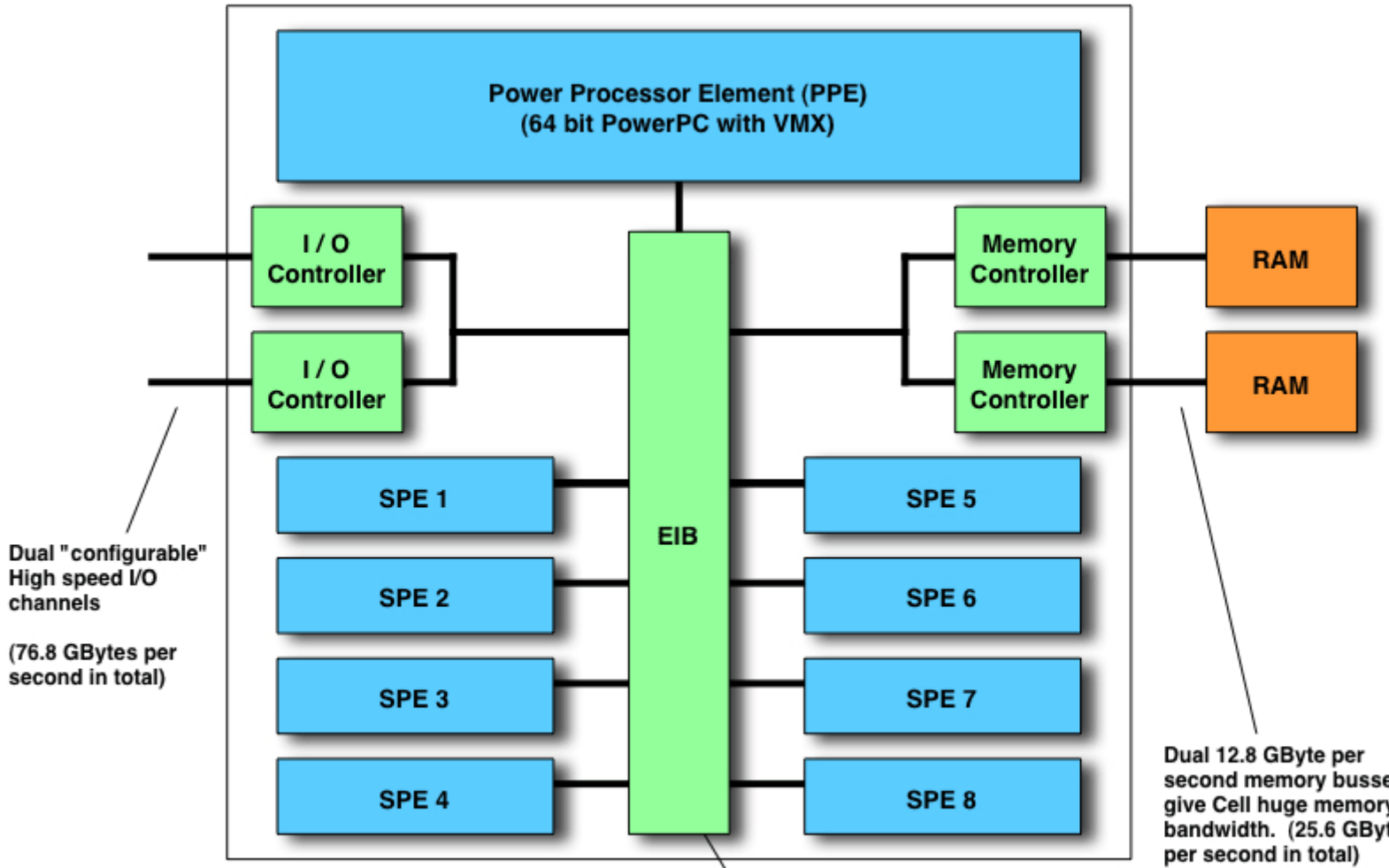
COMPUTER ENTERTAINMENT

TOSHIBA

IBM

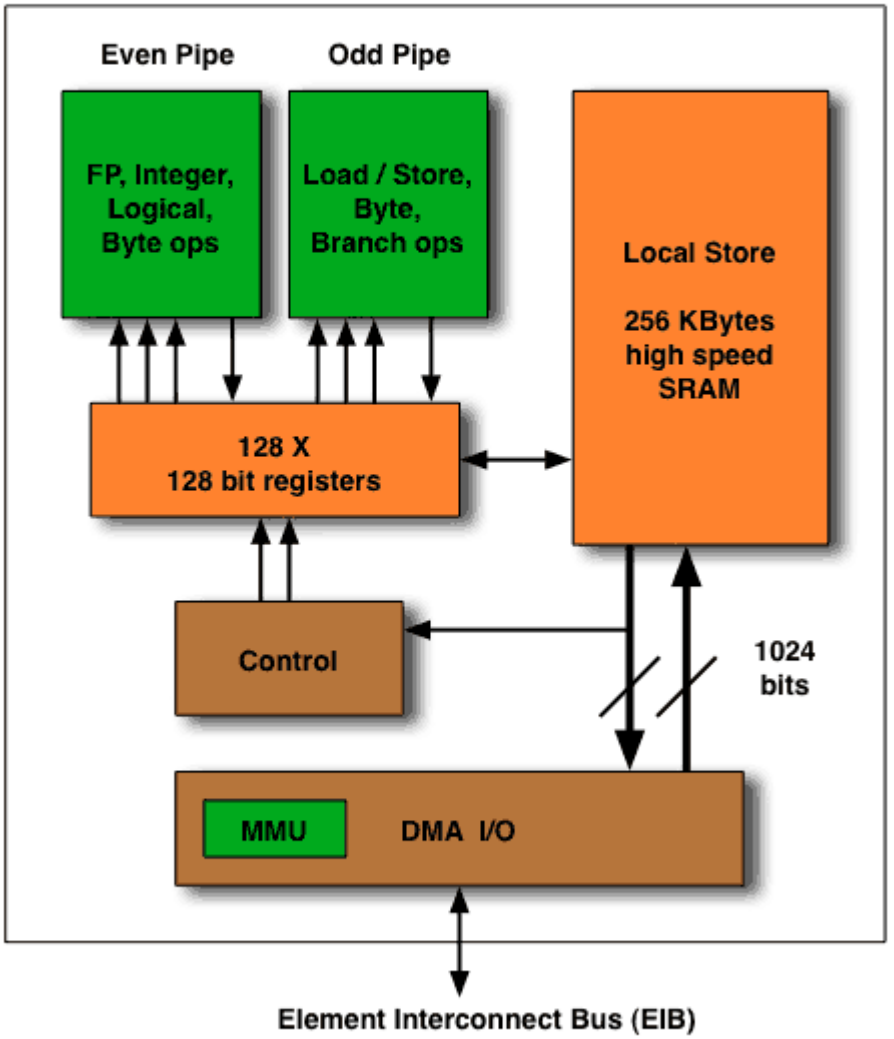
PLAYSTATION 3

Cell Processor Architecture



Cell SPE Architecture

Each SPE is an independent vector CPU
capable of 32 GFLOPs or 32 GOPs (32 bit @ 4GHz.)



Element Interconnect Bus (EIB)

- Communication bus connecting the on-chip elements including an arbitration unit (traffic light)
- Circular ring of four 16B wide unidirectional channels
  - Counter-rotate in pairs
  - Each channel can handle up to 3 transactions concurrently
  - Each participant on bus has a 16B read port and 16B write port
-

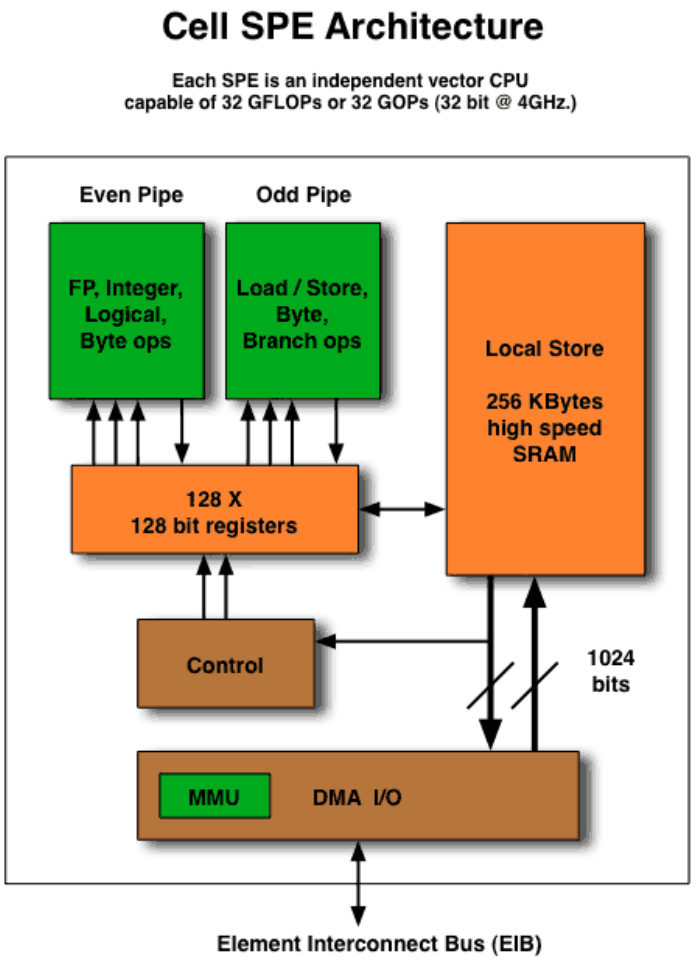
Flexibility of Cell's Resources

- Job Queue
  - PPE maintains job queue, schedules jobs in SPEs, monitors progress
  - SPE runs “mini kernel” to fetch and execute job and synch with PPE
- Self-multitasking of SPEs
  - Kernel and scheduling distributed across SPEs
  - Task synchronization done via mutexes or semaphores
- Stream Processing
  - Each SPE runs a distinct program

Memory Hierarchy: PPE

- PPE – Power Processor Element
- Caches:
  - Instruction Cache: 32K; 2-way set associative
  - L1 Cache: 32K; 4-way set associative
  - L2 Cache: 512K; 8-way set associative
- Contains Memory Management Units for accessing memory

Memory Hierarchy: SPE



- SPE - Synergistic Processor Element
- Vector CPU
- Local Store: 256K, each,
- Contain Memory Management Units, rather than coherency mechanism

Memory Hierarchy: XDR Interface

- Cell's DRAM interface
- Dual channel Rambus XIO macro which interfaces to Rambus XDR memory
- Each channel is 36-bits wide
- Cell's XDR memory bus runs at 400MHz
- 3.2GHz data signaling rates => memory bandwidth of 25.6GB/s

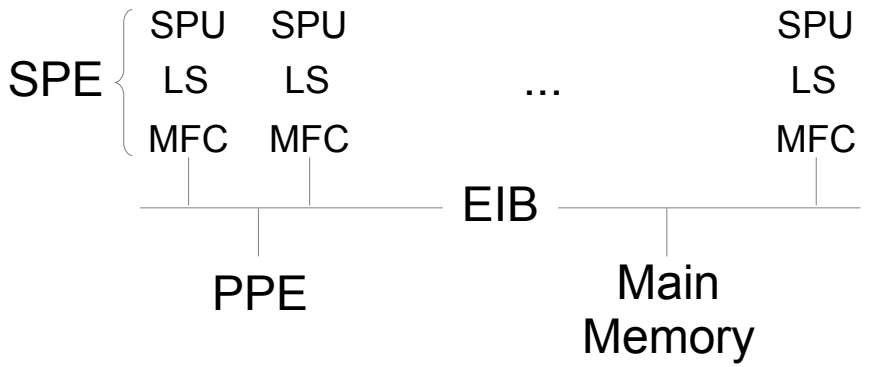
PPE Microarchitecture

- Out of order execution
- Dynamic branch prediction
  - Specialized “branch processor” exposes control of branching and branch prediction to the software
- 32k L1 D$, 32k L1 I$, 512k L2
- VMX unit – SIMD floating point (not part of the SPE!)

SPE Microarchitecture

- Static branch prediction
- Dual issue – one compute, one memory instruction per cycle
- No cache – not really needed
- 128 registers

Synergistic Processor Unit (SPU) ISA



- SPU ISA != PPE ISA (VMX)
- Vector instructions
- ½ the power, ½ the area, same performance
  - no cache: local store
  - no branch prediction: hint-for-branch

Questions?

References

Cell Architecture Explained, Version 2:

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