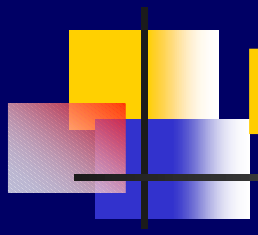
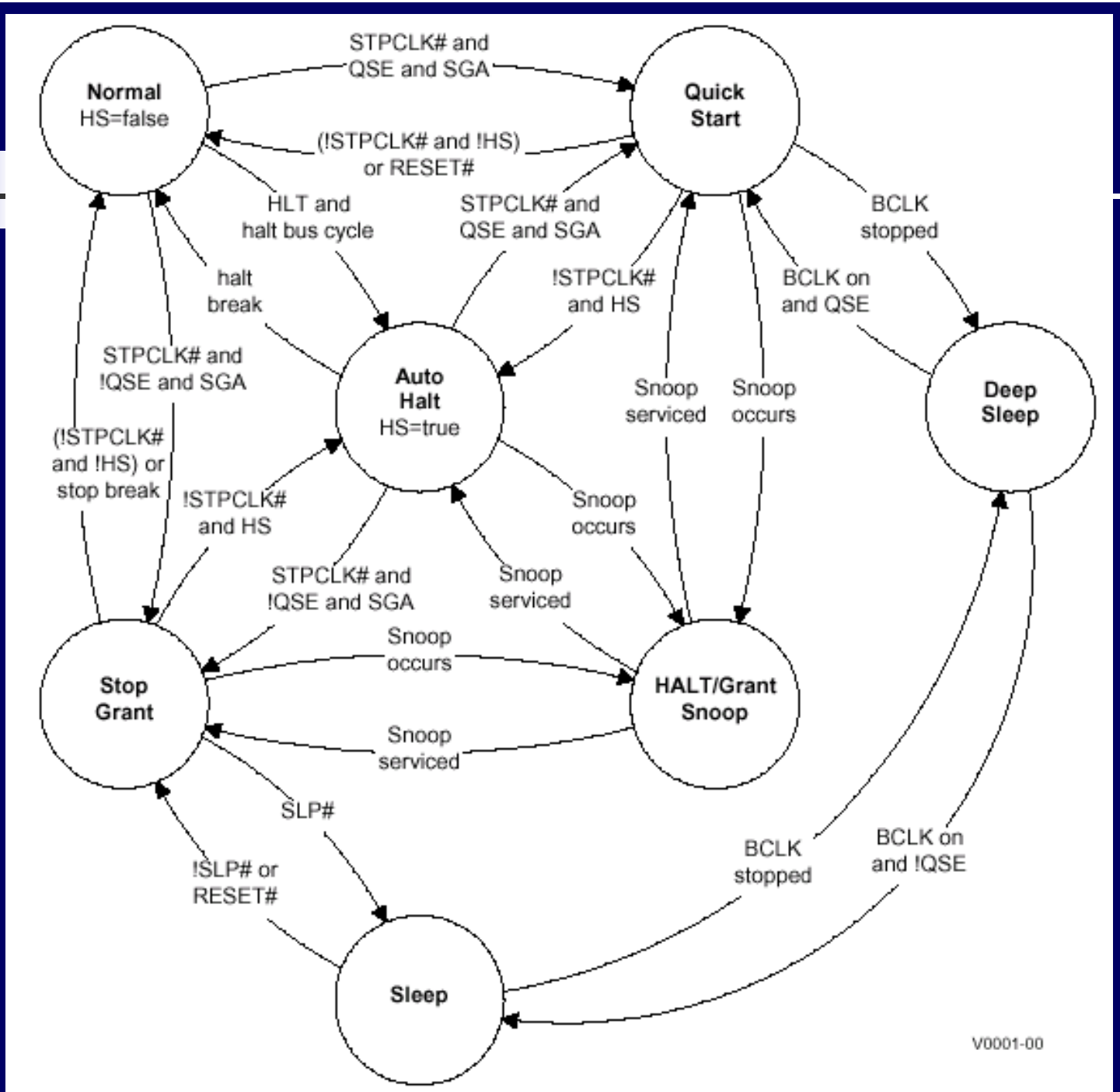


PIII Data Stream

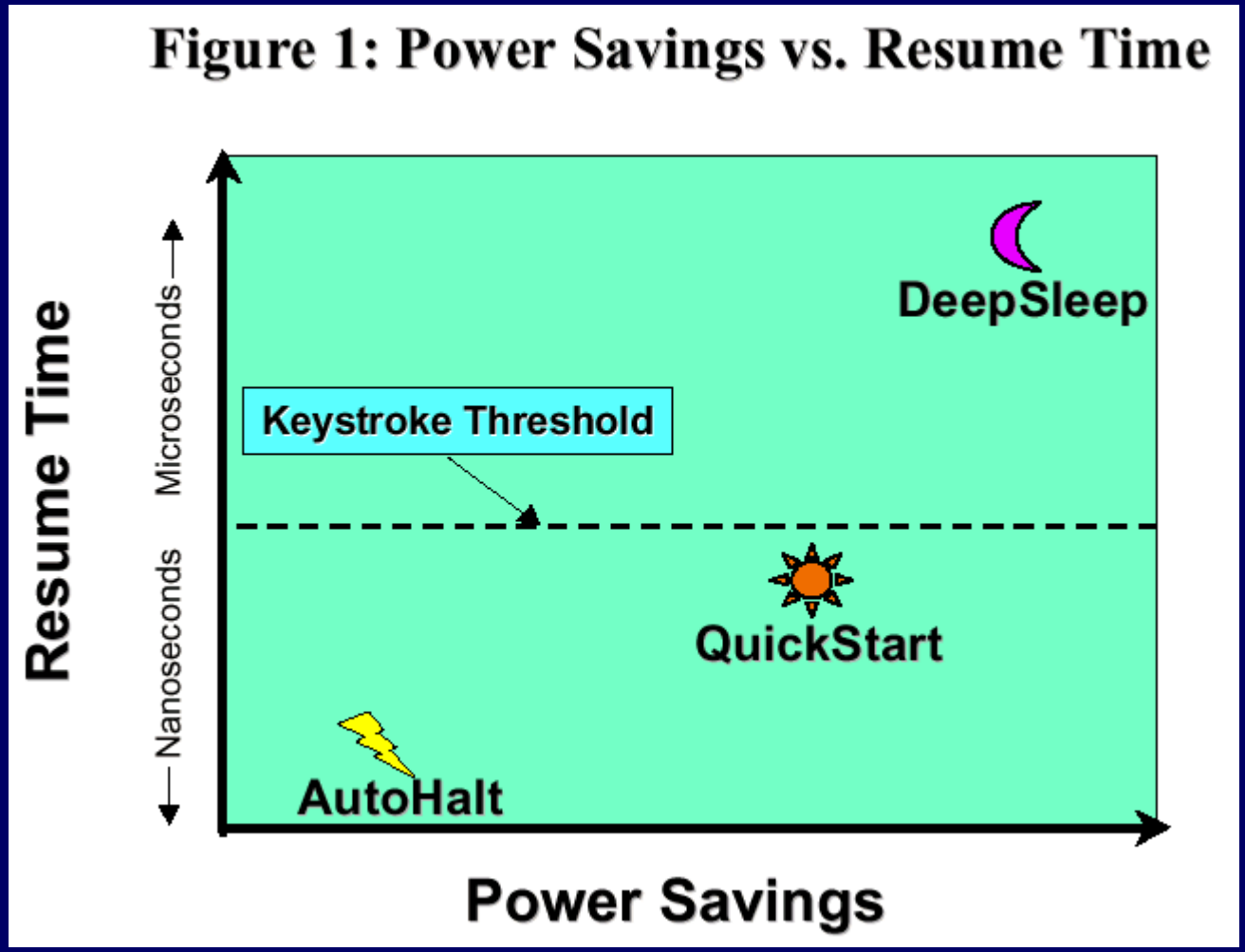
- Power Saving Modes
- Buses
  - System
  - Cache
- Memory Order Buffer
- Memory Hierarchy
  - L1 Cache
  - L2 Cache

Power Saving Modes

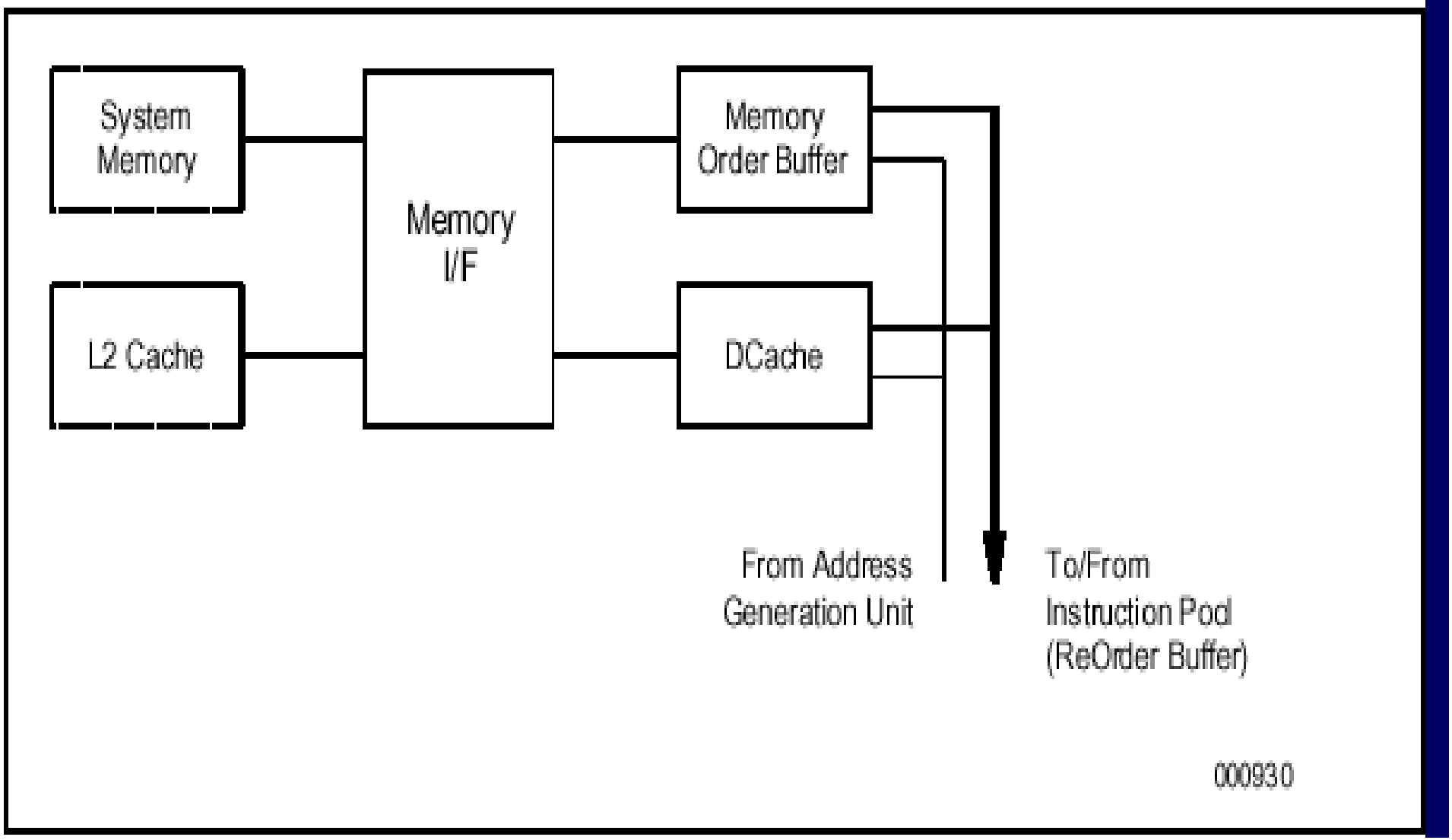
Clock State	Exit Latency	Snooping?	System Uses
Normal	N/A	Yes	Normal program execution
Auto Halt	Approximately 10 bus clocks	Yes	S/W controlled entry idle mode
Stop Grant	10 bus clocks	Yes	H/W controlled entry/exit mobile throttling
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 8 bus clocks	Yes	H/W controlled entry/exit mobile throttling
HALT/Grant Snoop	A few bus clocks after the end of snoop activity	Yes	Supports snooping in the low power states
Sleep	To Stop Grant state 10 bus clocks	No	H/W controlled entry/exit desktop idle mode support
Deep Sleep	30 µsec	No	H/W controlled entry/exit mobile powered-on suspend support


Normal
HS=false
Quick
Start
Auto
Halt
HS=true
Deep
Sleep
Stop
Grant
HALT/Grant
Snoop
Sleep
STPCLK# and
QSE and SGA
(!STPCLK# and !HS)
or RESET#
HLT and
halt bus cycle
halt
break
STPCLK# and
QSE and SGA
!STPCLK#
and HS
BCLK
stopped
BCLK on
and QSE
STPCLK# and
!QSE and SGA
(!STPCLK#
and !HS) or
stop break
!STPCLK#
and HS
Snoop
serviced
Snoop
occurs
Snoop
occurs
STPCLK# and
!QSE and SGA
Snoop
serviced
Snoop
occurs
Snoop
serviced
SLP#
!SLP# or
RESET#
BCLK
stopped
BCLK on
and !QSE
V0001-00

Power Saving Modes

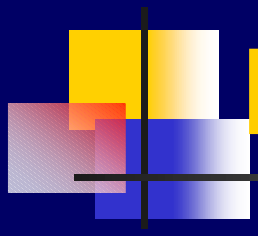


Bus Interface



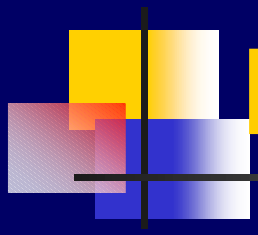
PIII Buses At-a-Glance

Address Bus Width	36 Bit
Data Bus Width	64 Bit
Dual Independent Bus (DIB) dedicated for L2	64+8 Bit (0.25 µm) 256+32 Bit (0.18 µm)



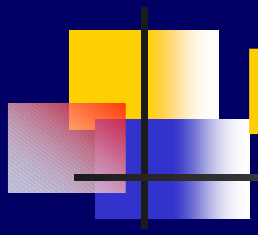
PIII System Bus

- 133 MHZ
- ECC error checking
- Supports multiple processors
- 4 write back buffers
- 6 fill buffers
- 8 bus queue entries



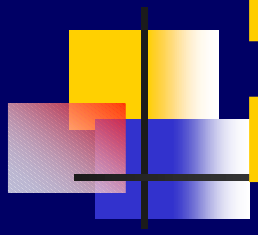
PIII Bus Enhancements

- Pentium II Write Buffers
- Removed dead cycle
- Using all fill buffers as WC fill buffers



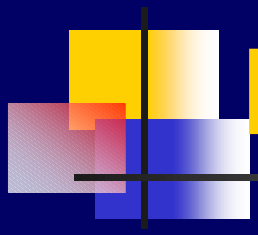
Memory Order Buffer (MOB)

- Load Buffer (LB)
  - 16 entries
- Store Buffer (SB)
  - 12 entries
- Re-dispatches μops
- Cache bandwidth



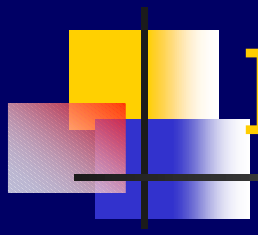
Memory Order Buffer (MOB) Re-Ordering

- Stores can not pass other loads or stores
- Loads can pass other loads, but can not pass stores
- Store Coloring
- Multiprocessing dilemma



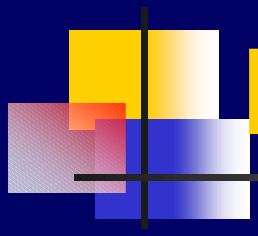
PIII Cache Design

- Harvard Architecture for L1
- Unified for L2
- Inclusive



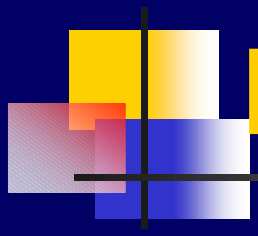
Inclusive vs. Exclusive

- Inclusive: reduces effective size of lower level caches
- Exclusive: data resides in one cache



L1 Instruction Cache

- Non-blocking 16 KB
- 4-way associativity
- 32 Byte/Line
- SI
- Fetch Port
- Internal and External Snoop Port
- Least Recently Used

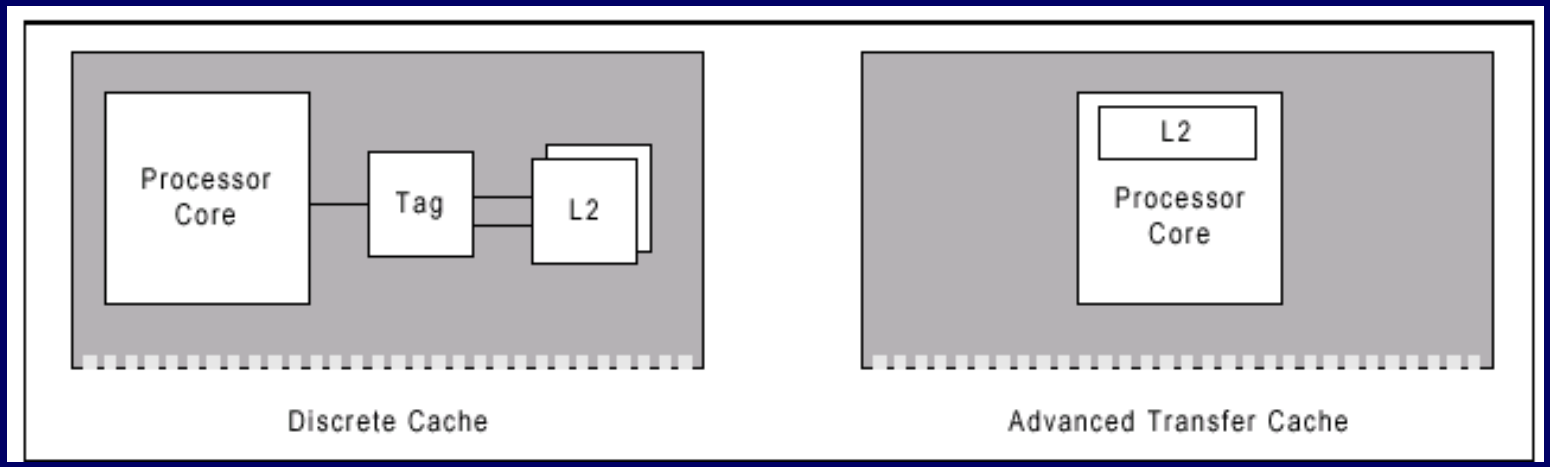


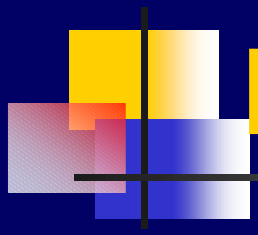
L1 Data Cache

- Non-blocking 16 KB
- 4-way associativity
- 32 Bytes/Line
- MESI
- Dual-ported
- Snoop Port Write Allocate
- Least Recently Used

L2 Cache

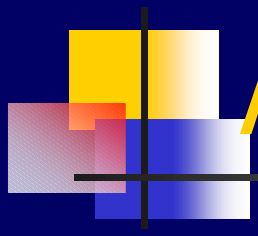
- Discrete Level 2 Cache
- Advanced Transfer Cache





Discrete L2 Cache

- 512 KB+ off-die
- 64 Bit bus
- 4-way set associativity
- Slower, but bigger

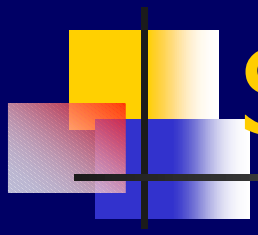


Advanced Transfer Cache

- 256 KB on-die
- 256 Bit Bus
- 8-way associativity
- Faster, but smaller

L2 Cache Effects on Power

Proc. Core Freq. (MHz)	L2 Cache Size (Kbytes)	Thermal Design Power[2] (W)	L2 Cache Power (W)	Power Density[4] (W/cm^2) Up to CPUID 0683h	Power Density[4] (W/cm^2) For CPUID 0686h[6]	Max $T_{JUNCTION}$ (°C)	$T_{JUNCTION}$ Offset[3] (°C)	L2 Cache Min T_{CASE} (°C)	L2 Cache Max T_{CASE} (°C)	Min T_{COVER} (°C)	Max T_{COVER} (°C)
450	512	25.3	1.26	21.6[5]	n/a	90	4.8	5	105	5	75
500	512	28.0	1.33	23.9[5]	n/a	90	4.8	5	105	5	75
533B	512	29.7	1.37	25.4[5]	n/a	90	4.8	5	105	5	75
533EB	256	14.0	N/A	19.3[6]	22.0	82	2.0[7]	N/A	N/A	5	75
550	512	30.8	1.37	26.3[5]	n/a	80	4.8	5	105	5	75
550E	256	14.5	N/A	20.0[6]	22.8	82	2.1[7]	N/A	N/A	5	75
600	512	34.5	1.60	29.5[5]	n/a	85	4.8	5	105	5	75
600B	512	34.5	1.60	29.5[5]	n/a	85	4.8	5	105	5	75
600E	256	15.8	N/A	21.8[6]	24.8	82	2.3[7]	N/A	N/A	5	75
600EB	256	15.8	N/A	21.8[6]	24.8	82	2.3[7]	N/A	N/A	5	75
650	256	17.0	N/A	23.4[6]	26.7	82	2.5[7]	N/A	N/A	5	75
667	256	17.5	N/A	24.1[6]	27.5	82	2.5[7]	N/A	N/A	5	75
700	256	18.3	N/A	25.2[6]	28.7	80	2.7[7]	N/A	N/A	5	75
733	256	19.1	N/A	26.3[6]	30.0	80	2.8[7]	N/A	N/A	5	75
750	256	19.5	N/A	26.9[6]	30.6	80	2.8[7]	N/A	N/A	5	75



Software Controlled Caching

- Streaming Data Trashes Cache
- Skip levels in Memory Hierarchy
- Senior Load